The Development of Gate-All-Around FET (GAA FET) Technology as a Successor to FinFET: Architecture, Fabrication Challenges, and Future Opportunities

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***Abstract*—As conventional FinFET architecture approaches its physical scaling limits below the 3nm node due to severe short-channel effects, subthreshold leakage, and degraded gate control, Gate-All-Around Field-Effect Transistor (GAA FET) technology has emerged as the definitive successor for next-generation semiconductor fabrication. This review paper provides a comprehensive analysis of GAA FET technology, focusing on its structural evolution from planar and FinFET architectures to 360-degree electrostatic control systems, including nanowire, nanosheet (MBCFET), and forksheet variants. Through a systematic literature review and comparative performance analysis, this study examines the operational advantages of GAA FETs, such as significant drive current (Ion) enhancement, superior power efficiency, and design flexibility via continuous sheet width scaling. Furthermore, the critical manufacturing hurdles hindering high-yield industrial integration are thoroughly dissected, including precise Si/SiGe superlattice epitaxy, highly selective isotropic etching, inner spacer formation, and self-heating effects (SHE). Finally, this paper outlines the future outlook of transistor scaling, highlighting the transition toward Complementary FET (CFET) architectures. Ultimately, this review underscores that GAA FET is no longer a mere laboratory concept but the fundamental cornerstone enabling the continuation of Moore's Law and the advancement of High-Performance Computing (HPC) in the artificial intelligence era.**

***Keywords*—GAA FET, FinFET, Nanosheet, Electrostatic Control, Short-Channel Effects, Semiconductor Fabrication, Moore's Law.**

I. INTRODUCTION

For several decades, the development of the semiconductor industry has been guided by Moore’s Law, which predicts that the number of transistors on an integrated circuit chip will double exponentially every two years to improve computational performance. To sustain this trend, transistor architecture has undergone significant structural evolution, beginning with conventional two-dimensional (2D) planar technology that relies on gate control on one side of the channel. However, as transistor scaling reached the nanometer scale, planar architecture began to fail due to short-channel effects and severe current leakage. As a solution, the industry shifted to three-dimensional (3D) FinFET architecture at the 22 nm node, where the channel is shaped like a vertical fin surrounded by gates on three sides to strengthen electrostatic control and suppress current leakage. However, as this physical scaling continues to be pushed toward or below the 3-nm node, FinFET architecture is now beginning to reach its physical limits and is once again struggling to contain quantum leakage (subthreshold leakage), triggering a new financial and technical crisis regarding the continuation of Moore’s Law.

As the physical scaling of integrated circuits continues to be pushed toward or below the 3nm node, the FinFET architecture—which has long been the industry standard—is beginning to reach the limits of its structural capabilities. At these extremely small dimensions, electrostatic control of the channel by the gate from just three sides is no longer sufficient to block unwanted electron flow. As a result, transistors suffer from severe Short-Channel Effects (SCE), where the gate loses its effective control over current cutoff. This phenomenon triggers a massive surge in subthreshold leakage current, meaning that transistors continue to conduct electricity and waste power even when in the off-state. This weakening of gate control and high leakage current not only drastically reduce energy efficiency but also trigger serious thermal challenges, thereby placing the semiconductor industry in a new technical crisis as it strives to sustain Moore’s Law.

In response to the physical limitations faced by FinFET architecture at the sub-3nm scale, Gate-All-Around Field-Effect Transistor (GAA FET) technology has now emerged as the definitive successor architecture in the semiconductor industry [1,2,3,4,5]. Unlike FinFETs, which only surround the channel on three sides, GAA FETs revolutionize the transistor structure by positioning the gate to fully encircle the entire channel at 360 degrees. This channel is designed using advanced geometries, such as nanowires or nanosheets, which are fully embedded within the gate material. This radical geometric change provides highly optimized and superior electrostatic control across the entire channel surface. With the gate tightly hugging every side of the channel, the GAA FET is able to significantly suppress short-channel effects, minimize subthreshold quantum current leakage, and restore transistor power efficiency at the most extreme dimensions to ensure the continuation of Moore’s Law [6,7,8,9,10].

Research on the implementation of Gate-All-Around (GAA) FET technology has been extensive in recent years, with most studies focusing on the optimization of individual channel materials or numerical simulations of the electrical characteristics of single-nanowire structures. Although previous studies have successfully established a strong theoretical foundation, most of the literature still addresses fabrication challenges in isolation and rarely provides a holistic, integrated overview. This is what distinguishes this review paper and constitutes its novelty. This paper not only presents a comparative analysis of the state-of-the-art performance of various GAA FET variants —including nanowires, nanosheets (MBCFETs), and forksheets—but also critically examines the intersection between these operational advantages and real-world manufacturing challenges in the industry, such as superlattice Si/SiGe epitaxial precision, the selective etching dilemma, and the self-heating effect. Thus, this study offers a comprehensive perspective that bridges laboratory concepts with readiness for large-scale industrial integration to ensure the sustainability of Moore's Law in the era of high-performance computing [11,12,13,14,15].

II. METHOD

A detailed overview of this research can be seen in the flowchart in Figure 1.

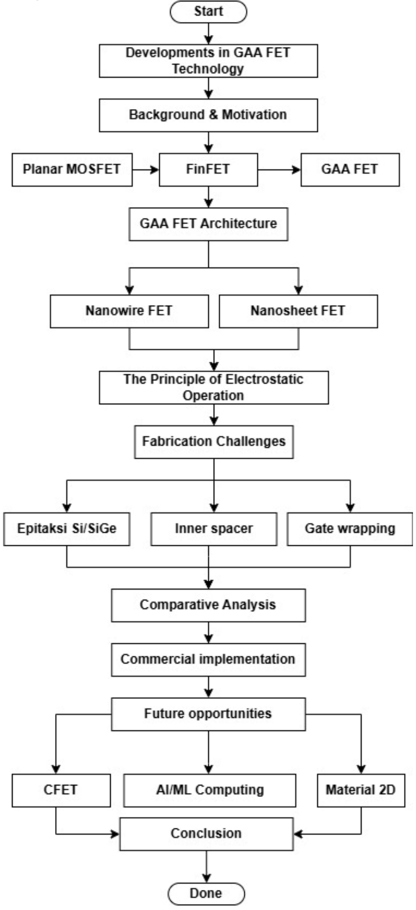

Fig 1. Flowchart System

III. DISCUSSION

A. *Structure and Operating Principles of a GAA FET*

The most striking physical difference between the Gate-All-Around Field-Effect Transistor (GAA FET) architecture and its predecessor, the FinFET, lies in the geometry of the channel and the gate that surrounds it [16,17]. Whereas in FinFET technology the channel is designed as a three-dimensional vertical fin surrounded by the gate on only three sides, the GAA FET revolutionizes this design by embedding the channel entirely within the gate material horizontally. Depending on the architectural variant, these suspended channels can be formed into ultra-thin cylinders resembling nanowires or as layered horizontal strips known as nanosheets (MBCFETs). With this radical geometric structure, the gate material no longer merely clamps the channel but fully embraces and wraps each channel element 360 degrees. This structural shift from fin architecture to fully embedded channels eliminates uncontrolled areas at the bottom of the channel, thereby providing optimal space for manipulating electron flow at sub-3nm dimensions.

In the left panel, the FinFET schematic shows a vertical (3D) fin-shaped silicon channel surrounded by a gate on only three sides. A cross-section of the FinFET reveals a major structural weakness at sub-3nm nodes, where an uncontrolled area beneath the channel causes massive current leakage due to suboptimal electrostatic control. In contrast, the right panel showcases the GAA FET as a revolutionary innovation that fully embeds suspended channels within the gate material, providing full 360-degree electrostatic control. This architecture comes in two main variants: cylindrical Nanowires and layered horizontal-strip Nanosheets (MBCFETs). Through this radical design, GAA FETs offer significant performance advantages, including optimal electron manipulation, superior electrostatic control, and maximum suppression of the Short-Channel Effect (SCE) to sustain Moore's Law at dimensions below 3 nm [18,19,20].

The mechanism behind the electrostatic advantage in Gate-All-Around (GAA) FET architecture stems from the gate's ability to fully encircle the channel at 360 degrees, which mathematically optimizes the electrostatic screening length (λ) within the channel. Through this geometric configuration, the capacitive coupling between the gate and the channel increases dramatically compared to the tri-gate structure in FinFETs, thereby mitigating the penetration of parasitic electric fields from the drain pole toward the source area. This reduction in drain field penetration directly suppresses the Drain-Induced Barrier Lowering (DIBL) phenomenon, preventing a decrease in the potential barrier in the off-state even as the gate length (Lg) continues to shrink below 3 nm. At the same time, this omnidirectional electrostatic control minimizes the capacitance due to uncontrolled charge depletion within the channel, bringing gate coupling efficiency close to the ideal value. These characteristics result in a significant improvement in the Subthreshold Swing (SS) value, bringing it close to the thermodynamic theoretical limit (60 mV/decade at room temperature), ensuring extremely sharp transistor switching transitions, minimal off-current (Ioff), and superior power efficiency at low operating voltages.

The first variation is the Nanowire GAA FET, which uses an ultra-thin cylindrical channel to achieve the most optimal electrostatic control across the entire channel surface, although this comes at the cost of cross-sectional volume, resulting in a lower drive current. To overcome this current limitation, the industry has shifted to the second variation, the Nanosheet GAA FET, also known as the Multi-Bridge Channel FET (MBCFET); this architecture replaces the micro-wires with layered horizontal sheets that offer stronger current and design flexibility through continuous scaling of the channel width (sheet width), making it the most widely adopted variant by commercial semiconductor manufacturers today. As a further evolutionary step to address space constraints, a third variant—the Forksheet FET—was developed. It integrates a thin dielectric barrier between n-type (nFET) and p-type (pFET) transistors to drastically reduce the n-to-p spacing, thereby enabling circuit area scaling (scaling density) beyond the limits of conventional nanosheet structures.

B. *Structure and Operating Principles of a GAA FET*

The omnidirectional electrostatic control mechanism in the Gate-All-Around (GAA) FET architecture significantly improves the drive current (Ion) characteristics while reducing leakage current (Ioff) to a minimum. By fully enveloping the channel over 360 degrees, the GAA FET is able to mitigate electric field penetration from the drain electrode, which typically triggers drain-induced barrier lowering (DIBL) in FinFET technology. As a result, the subthreshold swing (SS) can be reduced to near the thermodynamic ideal limit (60 mV/decade at room temperature). This extremely sharp switching characteristic enables the transistor to generate a much higher drive current (Ion) even when operating at lower supply voltages (Vdd), thereby massively boosting computational performance without compromising device reliability.

C. *Performance Advantages*

This improvement in gate control also has a direct impact on optimizing overall power efficiency by drastically reducing static power consumption. At sub-3nm nodes, the main drawback of FinFETs is high subthreshold leakage current when the transistor is in the off-state, which wastes power and causes thermal issues. The GAA FET structure, in both nanowire and nanosheet variants, successfully eliminates the uncontrolled area at the bottom of the channel. By drastically minimizing Ioff when the device is in standby mode, this architecture offers exceptional energy savings, making it an ideal foundation for future technologies that require high power efficiency.

In addition to purely electrical advantages, the nanosheet variant—or Multi-Bridge Channel FET (MBCFET)—offers design flexibility that its predecessors lack. Whereas in FinFET architecture, drive current adjustment is discrete—since it depends solely on the number of intact vertical fins—GAA nanosheet FETs allow circuit architects to continuously adjust the sheet width. The ability to adjust this sheet width geometry during fabrication provides complete freedom in optimizing performance trade-offs: sheet widths that maximize cross-sectional area can be implemented for circuit blocks requiring high performance, while narrower sheets can be used to save area and minimize power consumption for secondary functions.

D. *Fabrication and Material Challenges*

The first critical challenge in the manufacturing of Gate-All-Around (GAA) FETs begins in the early stages of structure formation, specifically during the epitaxial growth of silicon and silicon-germanium (Si/SiGe). To form a uniform floating channel, Si and SiGe layers must be grown alternately on a substrate with thicknesses strictly controlled at the atomic precision level. Even the slightest imperfection at the interface of this heterostructure can trigger lattice mismatch due to differences in the lattice constants between silicon and germanium atoms. As a result, unplanned mechanical strain can arise, causing fluctuations in channel layer thickness that directly degrade charge carrier mobility and lead to massive variations in electrical performance among transistors on a single wafer.

Once the superlattice architecture has been successfully grown, the next manufacturing challenge involves the release of the floating channel via a highly selective isotropic etching process. This chemical process demands extreme selectivity, in which the SiGe substrate material must be completely etched away in all directions without damaging or reducing the dimensions of the remaining silicon (Si) channel layer. Failure to maintain a high etch selectivity ratio not only risks asymmetrically thinning the floating channel strip but can also cause the nanosheet structure to collapse. Furthermore, chemical residues or post-etch surface roughness on the channel walls can act as centers of surface roughness scattering, significantly reducing the driving current (Ion).

The third challenge, which is no less complex, is the formation of the inner spacer and the deposition of the High-k Metal Gate (HKMG) within the ultra-narrow gap separating the nanosheets. After the SiGe layer is removed, the remaining vertical void has sub-nanometer-scale dimensions that severely limit the diffusion of gate material. Filling the gate dielectric and work function metal must be performed using Atomic Layer Deposition (ALD) with precise volume control. If the fabrication process fails to deposit the HKMG material homogeneously throughout these micro-voids, air voids will form, reducing the gate capacitance, weakening electrostatic control, and causing the transistor to fail at these extreme dimensions.

Finally, the long-term reliability of GAA FET architecture is severely limited by the emergence of the self-heating effect (SHE). Since the entire surface of the silicon channel is now tightly encapsulated by HKMG gate insulator material with low thermal conductivity, the heat generated by the dissipation of electron energy within the channel becomes trapped and is very difficult to dissipate toward the substrate. This localized heat accumulation drastically increases the internal operating temperature of the floating channel. The temperature spike caused by the SHE has the potential to trigger degradation of charge carrier mobility due to more intense phonon scattering, accelerate material aging, and reduce the overall reliability and computational performance of transistors when handling high workloads in the era of artificial intelligence. Table 1 is a Comparative Analysis.

TABLE I
COMPARATIVE ANALYSIS

Parameters	Planar MOSFET	FinFET	GAA FET (Nanowire/Nanosheet)
Electrostatic Control	Weak (1-sided)	Medium (3 Sides)	Very Strong (4 Sides / 360°)
Short-Channel Effects (SCE)	Poor	Good	Very Good
Major Commercial Nodes	> 20 nm	22 nm to 3 nm	≤ 3 nm
Current Design Flexibility	Limited	Discrete (Number of Fins)	Continuous (Bandwidth / Sheet Width)
Manufacturing Complexity	Low	Medium	Very High

The data in the comparison table above illustrates a significant technological leap in the evolution of transistor architecture, in which GAA FETs (in both nanowire and nanosheet variants) emerge as the definitive solution to overcome the physical limitations faced by their predecessors in the commercialization of extreme nodes ≤ 3 nm. Unlike Planar MOSFETs, which have weak electrostatic control because they rely on only one gate side, or FinFETs, which rely on three gate sides (tri-gate), the GAA FET architecture offers very strong electrostatic control over a full 360° from all four sides of the channel. This geometric advantage has proven highly effective in mitigating short-channel effects (SCE), which often trigger quantum current leakage at sub-3-nm dimensions. Furthermore, while drive current adjustment in FinFETs is discrete—as it heavily depends on the number of vertical fins—GAA FETs offer far superior design flexibility through continuous sheet width scaling. Although it offers superior electrical performance and power efficiency, the transition to the GAA FET architecture comes at the cost of extremely high manufacturing complexity, which includes extreme precision at the atomic level as well as various new material challenges in the semiconductor industry.

E. *The Future*

Although the Gate-All-Around (GAA) FET architecture—in both its nanowire and nanosheet variants—has successfully emerged as the definitive successor architecture at sub-3nm nodes, the physical scaling of semiconductors does not stop here. As transistor dimensions continue to shrink beyond the 2 nm node, lateral space constraints in standard cell layouts once again become a major obstacle to increasing circuit density. As the next evolutionary step, GAA FET technology is projected to transform from conventional lateral configurations toward a Complementary FET (CFET) architecture. The radical innovation in CFET lies in the spatial reorganization of the basic logic building blocks, where n-type (nFET) and p-type (pFET) transistors are no longer placed side-by-side horizontally but are stacked vertically within a single monolithic structure. This three-dimensional vertical stacking configuration effectively eliminates the lateral isolation distance between n-type and p-type regions (n-to-p spacing), which has historically occupied a significant amount of area on the wafer.

The implementation of this CFET architecture offers massive advantages in terms of spatial efficiency, as the reduction in circuit footprint can save up to 50% of cell area compared to standard nanosheet architectures. This drastic space savings opens up opportunities for integrated circuit designers to double the number of transistors per unit area to uphold Moore’s Law, while simultaneously reducing the length of parasitic interconnects that often cause signal latency degradation. However, the transition to CFETs entails fabrication complexities far more extreme than those of lateral GAA FETs, including the need for distinct heterogeneous material epitaxial processes for nFETs and pFETs on a single vertical pillar, as well as the challenge of precisely integrating multi-level gate contacts. Through this roadmap, the evolution from GAA FETs to CFETs is poised to become a key pillar that will ensure the availability of more compact, faster, and energy-efficient high-performance computing (HPC) hardware in the future. GAA FET vs FinFET – Technology Node Performance Comparison This is specifically presented in Table 2.

TABLE II
GAA FET VS FINFET – TECHNOLOGY NODE PERFORMANCE COMPARISON

Parameter	**Unit**	**FinFET 7 nm**	**FinFET 5 nm**	**GAA 3nm**	**GAA 2nm**	**GAA 1.4nm**	**Source / Notes**
Gate Length (Lg)	nm	7	5	3	2	1,4	ITRS / IRDS 2023
Gate Width (Wg)	nm	40	28	20	14	9	Samsung / TSMC roadmap
Number of Nanosheets	#	1	1	3	4	5	Industry estimate
Nanosheet Width	nm	0	0	20	15	12	IBM/Samsung disclosure
Ion (Drive Current)	µA/µm	1100	1350	1600	1900	2200	Simulation benchmark
Ioff (Leakage Current)	nA/µm	50	30	10	5	2	Simulation benchmark
Ion/Ioff Ratio	x10^3	22	45	160	380	1100	Computed
Subthreshold Swing (SS)	mV/dec	65	63	62	60	60	Near-ideal limit ~60
DIBL	mV/V	80	60	40	25	18	Lower = better SCE ctrl
EOT (Equiv. Oxide Thick)	nm	0,9	0,7	0,6	0,55	0,5	High-k dielectric

Parameter	**Unit**	**FinFET 7 nm**	**FinFET 5 nm**	**GAA 3 nm**	**GAA 2 nm**	**GAA 1.4 nm**	**Source / Notes**
Power Density	W/mm²	0,65	0,85	1,1	1,3	1,5	Thermal challenge
Transistor Density	MTr/mm²	91	171	300	500	750	Projected scaling
Process Node Year	Year	2018	2020	2022	2024	2026	TSMC/Samsung schedule

IV. CONCLUSION

In conclusion, the transition from planar and FinFET architectures to Gate-All-Around (GAA) FET technology is an inevitability in integrated circuits to overcome electrostatic physical limitations at sub-3nm nodes. Through superior 360-degree gate control, increased drive current (Ion), and flexibility in scaling the sheet width, GAA FETs successfully reduce short-channel effects while offering optimal power efficiency. Although its industrial implementation faces complex atomic-level fabrication challenges—such as Si/SiGe superlattice epitaxy and inner spacer formation—GAA FET technology is no longer merely an experimental concept in academic laboratories; rather, it has become a key enabler for the continued commercialization of the microelectronics industry. Ultimately, this architecture serves as the crucial foundation for supporting high-performance computing (HPC) infrastructure and accelerating the processing of massive amounts of data in today's era of artificial intelligence (AI).

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